Conventional Wafer Test Example

Figure 1A

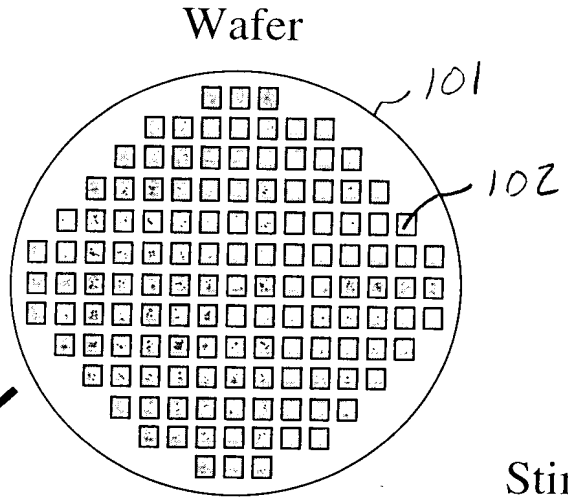


Figure 1B

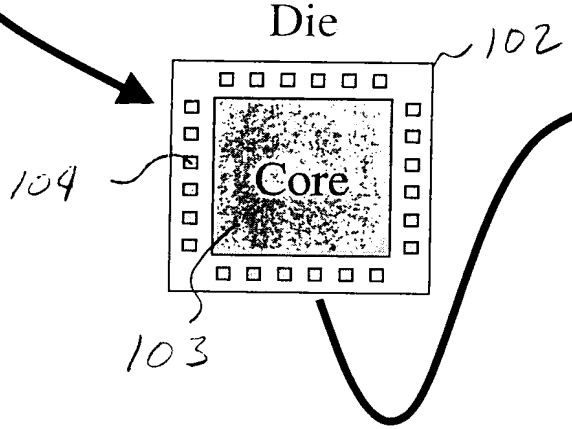
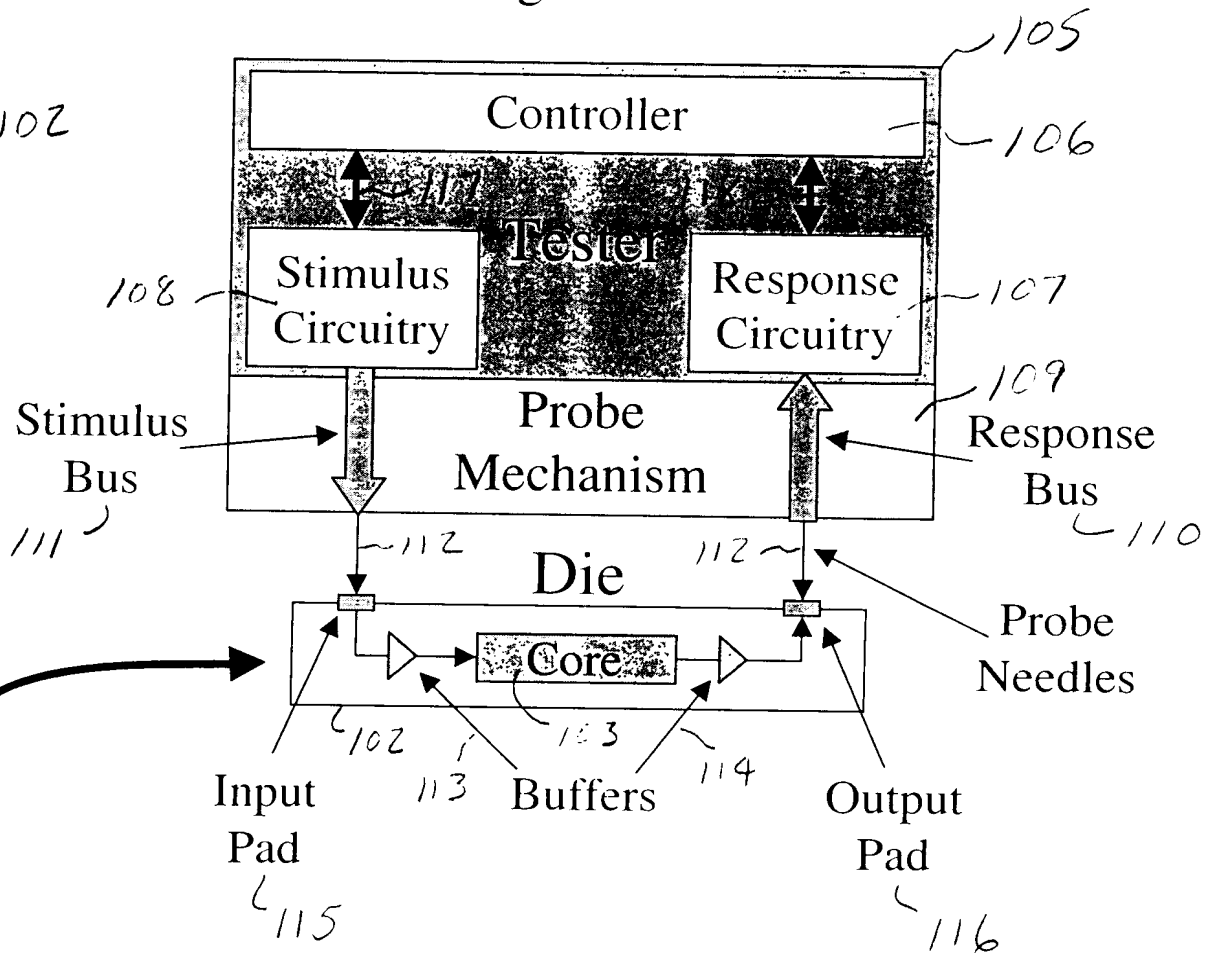
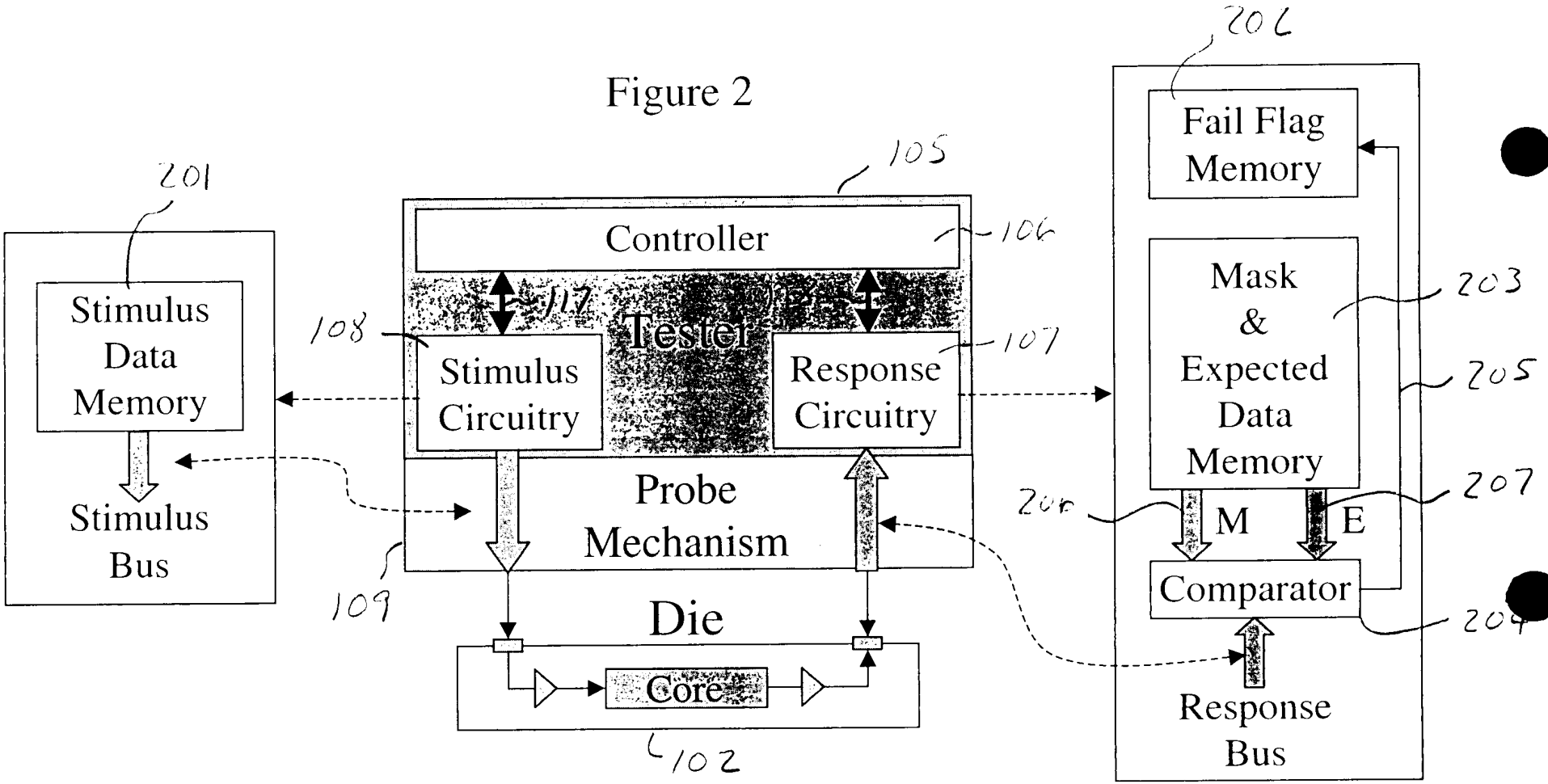


Figure 1C



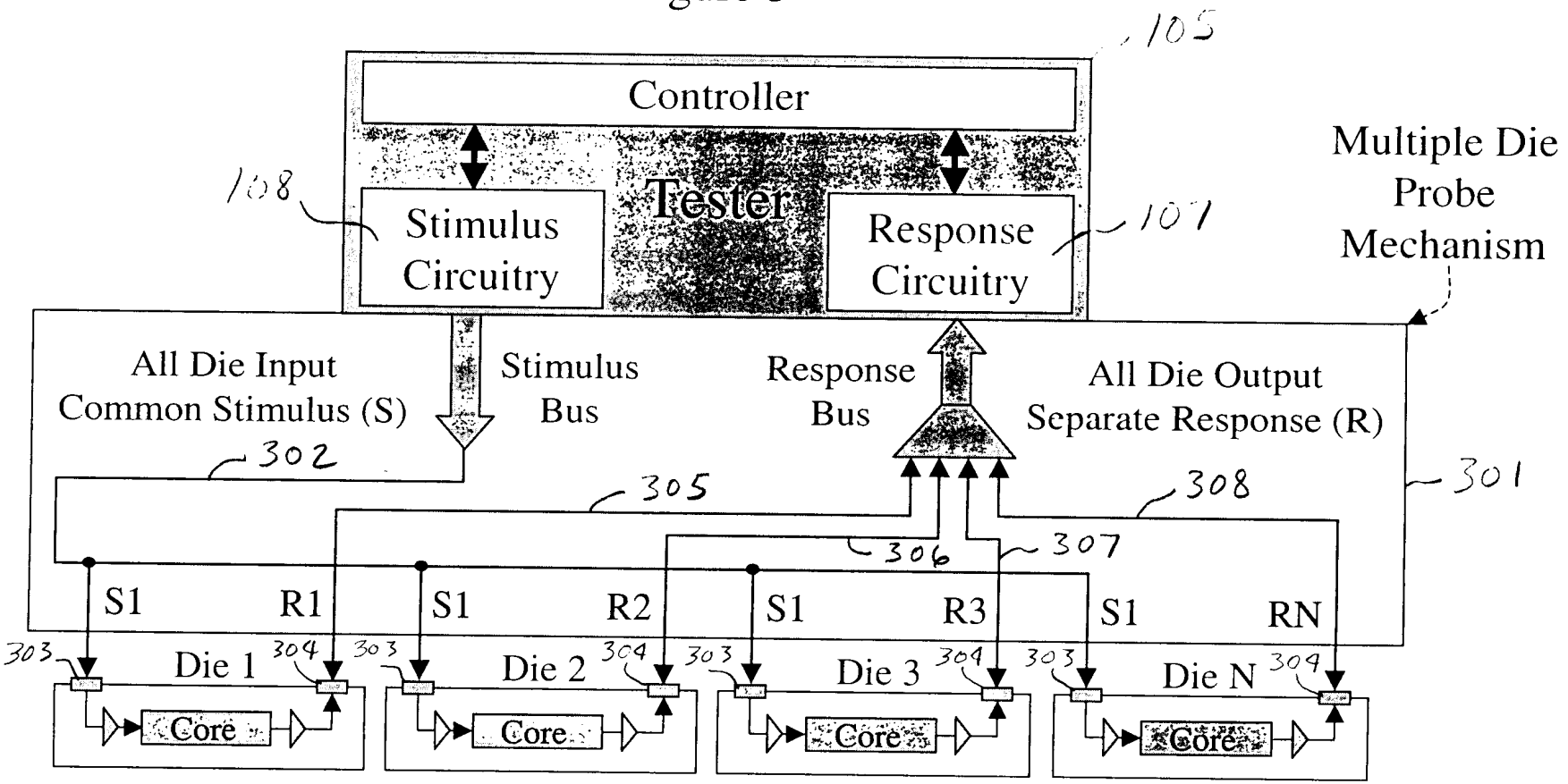
Conventional Tester
Stimulus & Response Circuitry

Figure 2



Multiple Die Probe Test Example

Figure 3



(Sum of R1-RN) <= (Tester Response Bus Width)

Figure 4

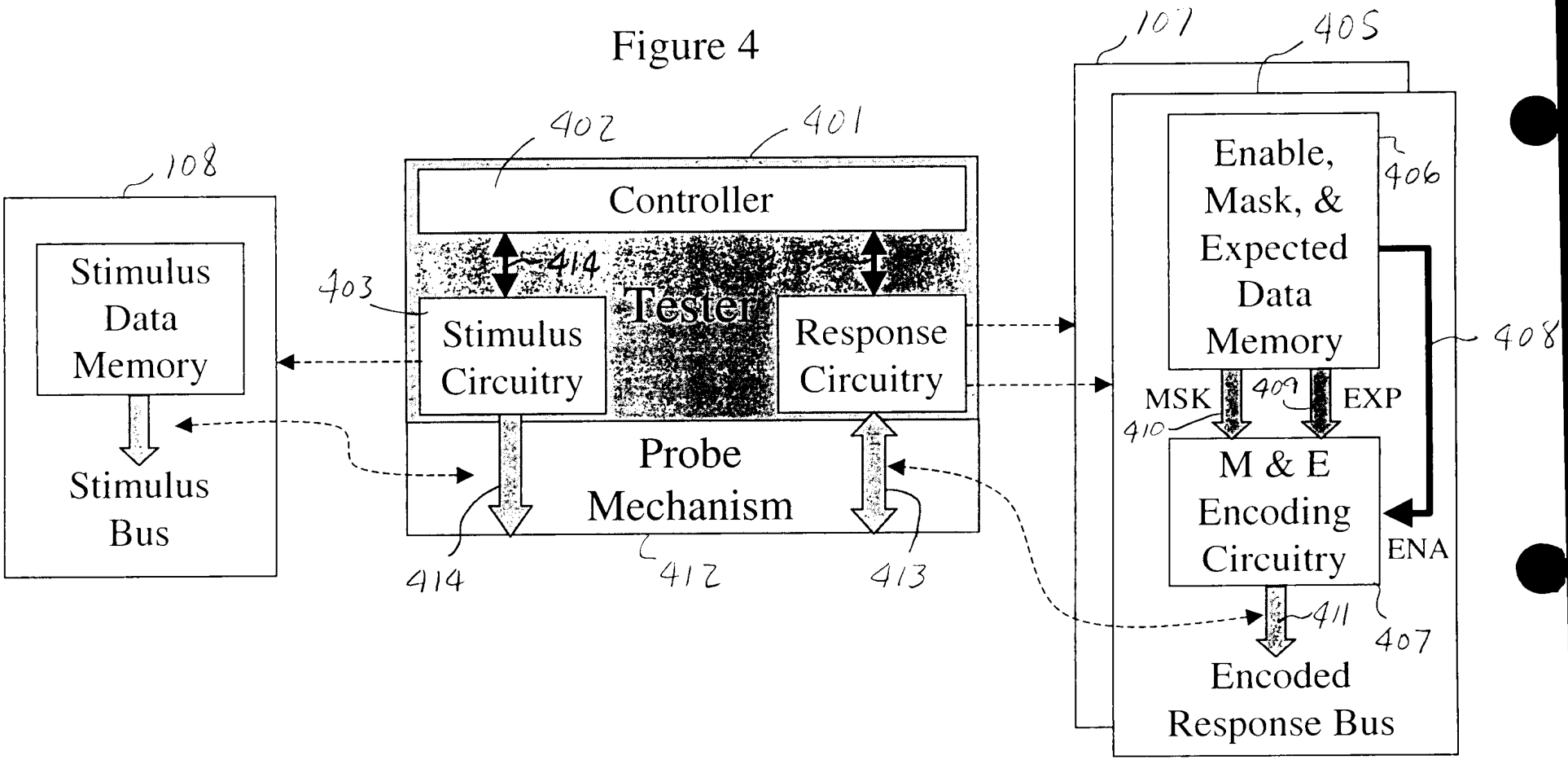

108
Stimulus Data Memory
Stimulus Bus
402
401
Controller
414
403
Stimulus Circuitry
Tester
Response Circuitry
Probe Mechanism
414
412
413
107
405
Enable, Mask, & Expected Data Memory
406
408
MSK
409
EXP
410
M & E Encoding Circuitry
ENA
411
407
Encoded Response Bus

Figure 5A

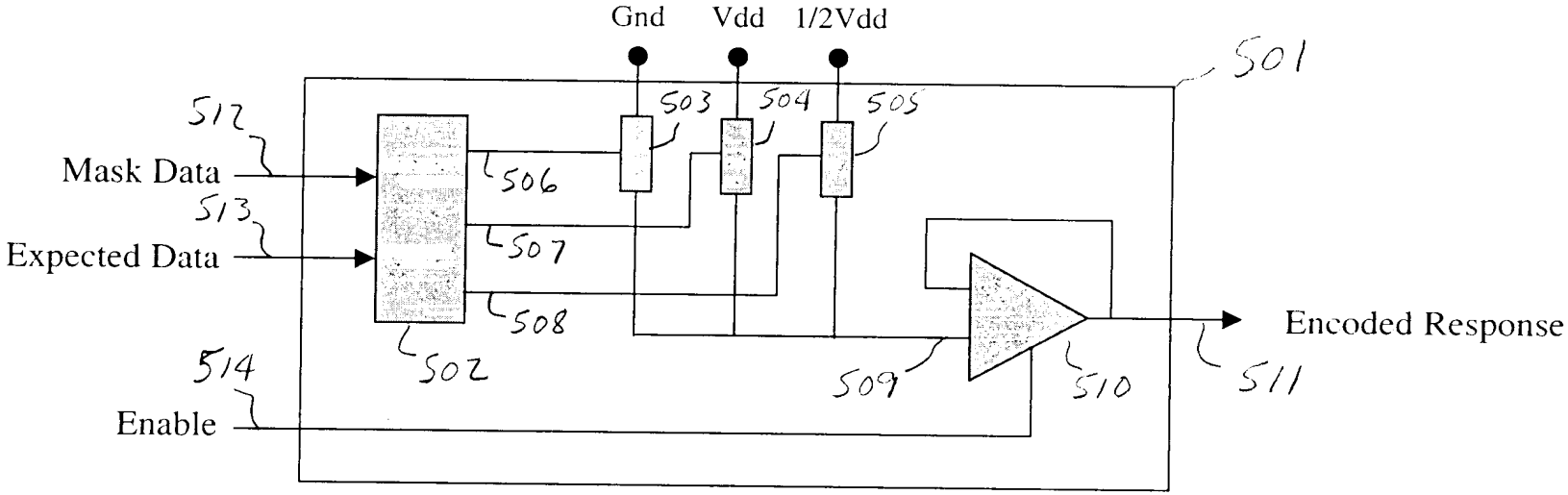


Figure 5B

ENA	MSK	EXP	ENR	Output Mode
0	0	0	Z	Disabled
1	0	0	Gnd	Low
1	0	1	Vdd	High
1	1	X	1/2Vdd	Mask

Figure 6A

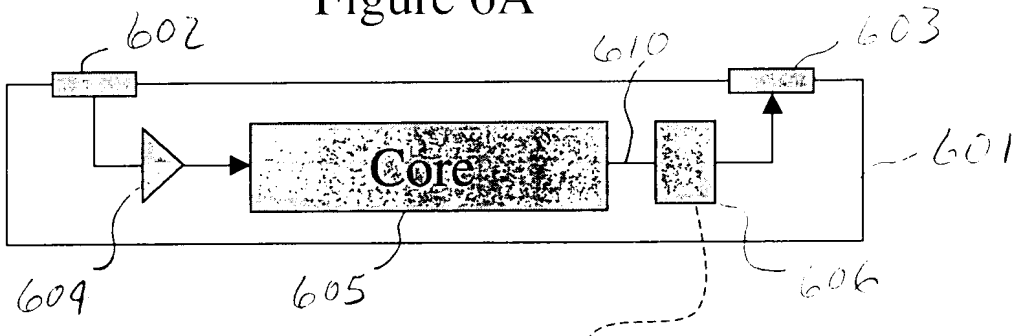
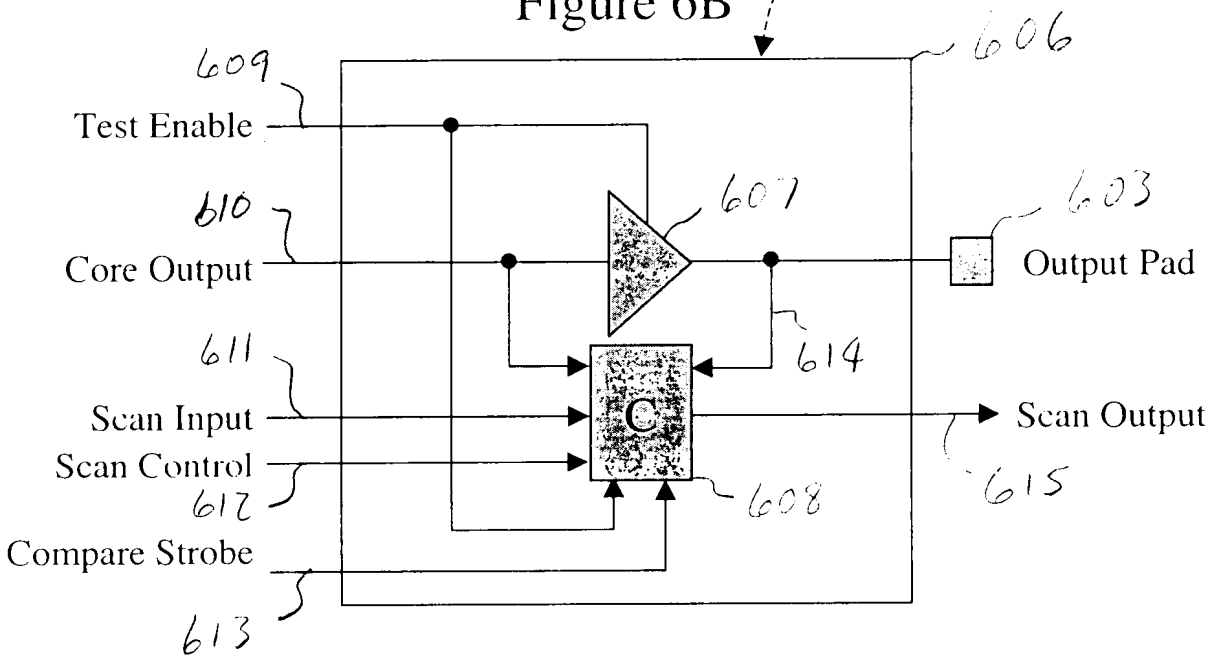


Figure 6B



Maskable Comparator For 2-State Outputs

Figure 7A

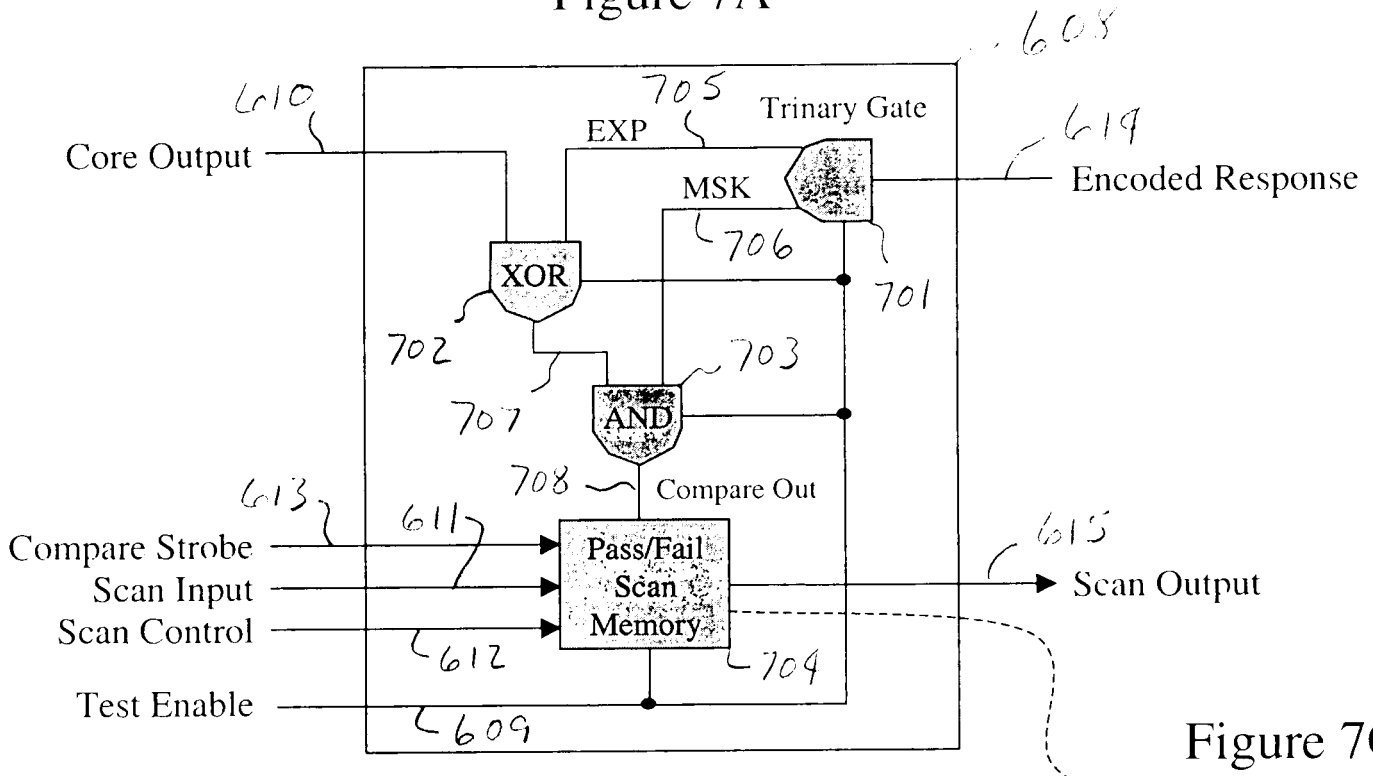
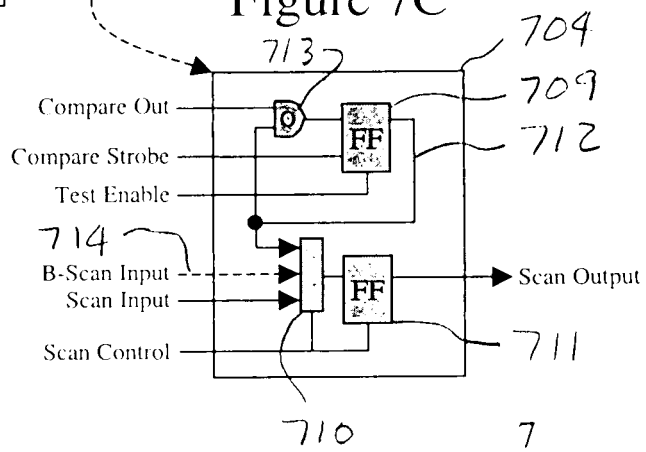


Figure 7B

TEN	ENR	MSK	EXP	Function Performed
0	X	X	X	Test Disabled
1	Gnd	1	0	Compare Low
1	Vdd	1	1	Compare High
1	1/2Vdd	0	X	Mask Compare

Figure 7C



Trinary Gate Circuit Example

Figure 8A

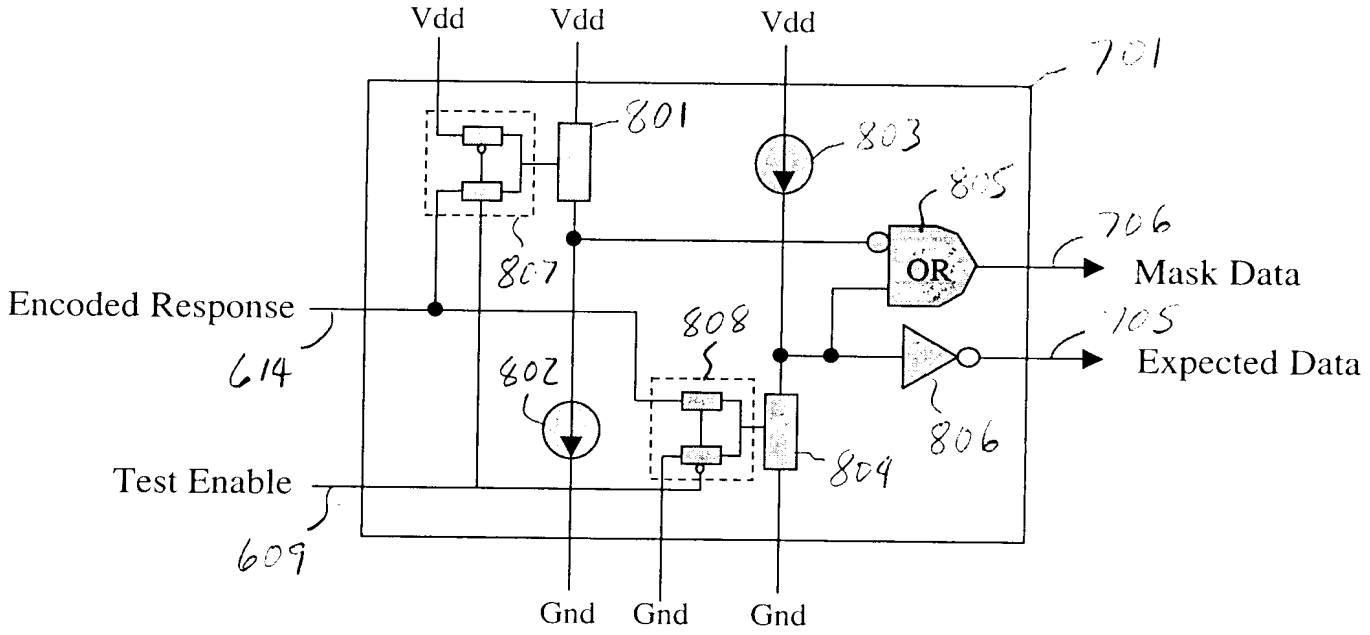


Figure 8B

TEN	ENR	MSK	EXP	Function Performed
0	X	1	0	Gate Disabled
1	Gnd	1	0	Output a Low
1	Vdd	1	1	Output a High
1	1/2Vdd	0	X	Output a Mask

Adapting Die 3-State Outputs
To Support Improved Wafer Testing

Figure 9A

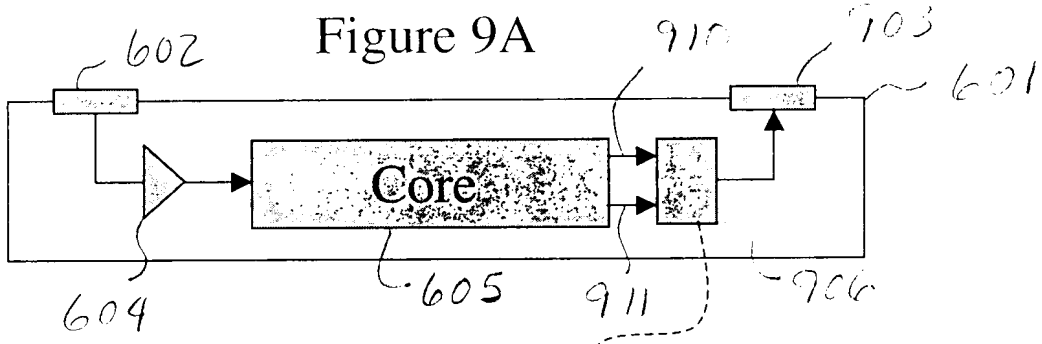
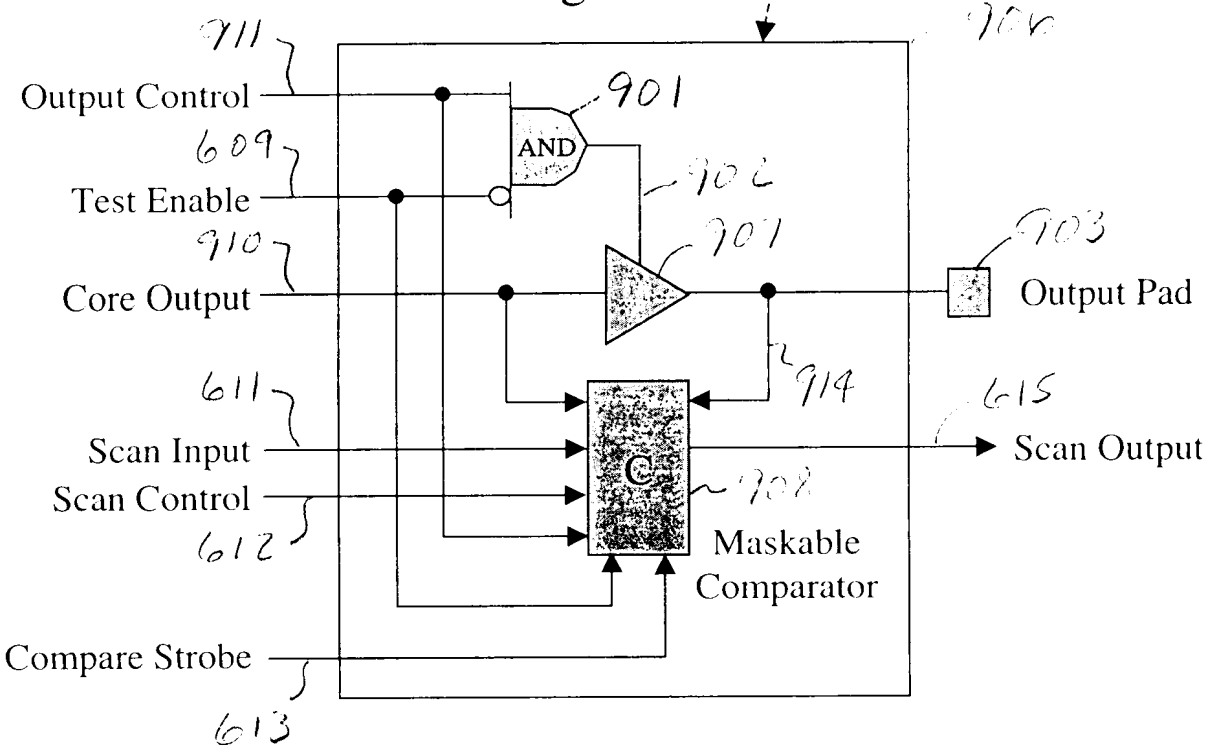


Figure 9B



Maskable Comparator For 3-State Outputs

Figure 10A

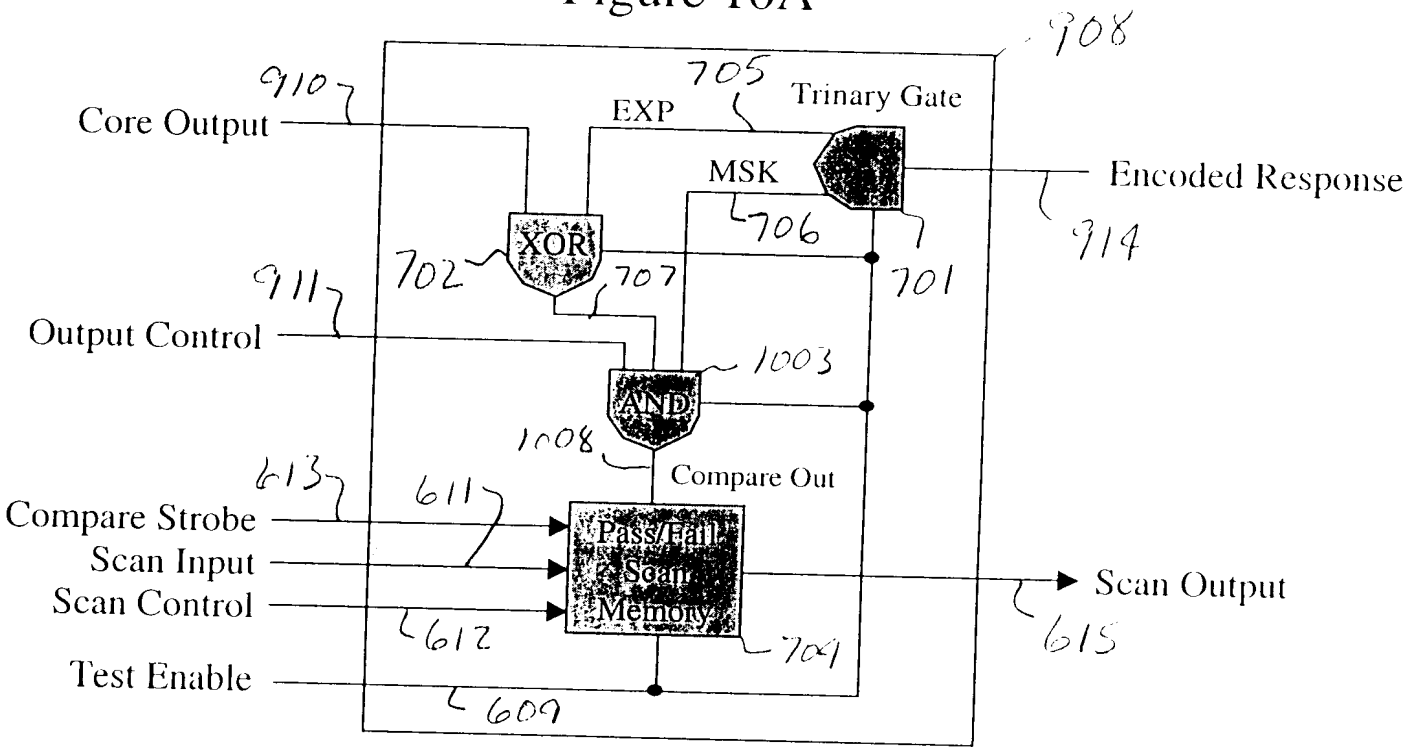


Figure 10B

OC	TEN	ENR	MSK	EXP	Function Performed
X	0	X	X	X	Test Disabled
1	1	Gnd	1	0	Compare Low
1	1	Vdd	1	1	Compare High
1	1	1/2Vdd	0	X	Mask Compare
0	1	Gnd/Vdd	1	0/1	Test Output Control

Adapting Die Input/Outputs
To Support Improved Wafer Testing

Figure 11A

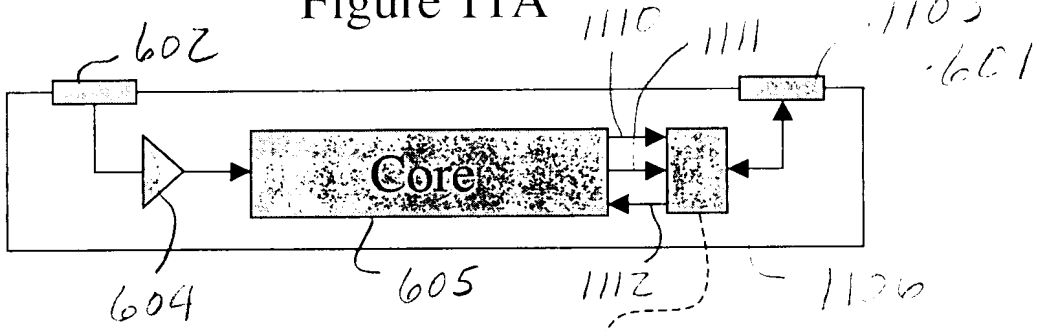
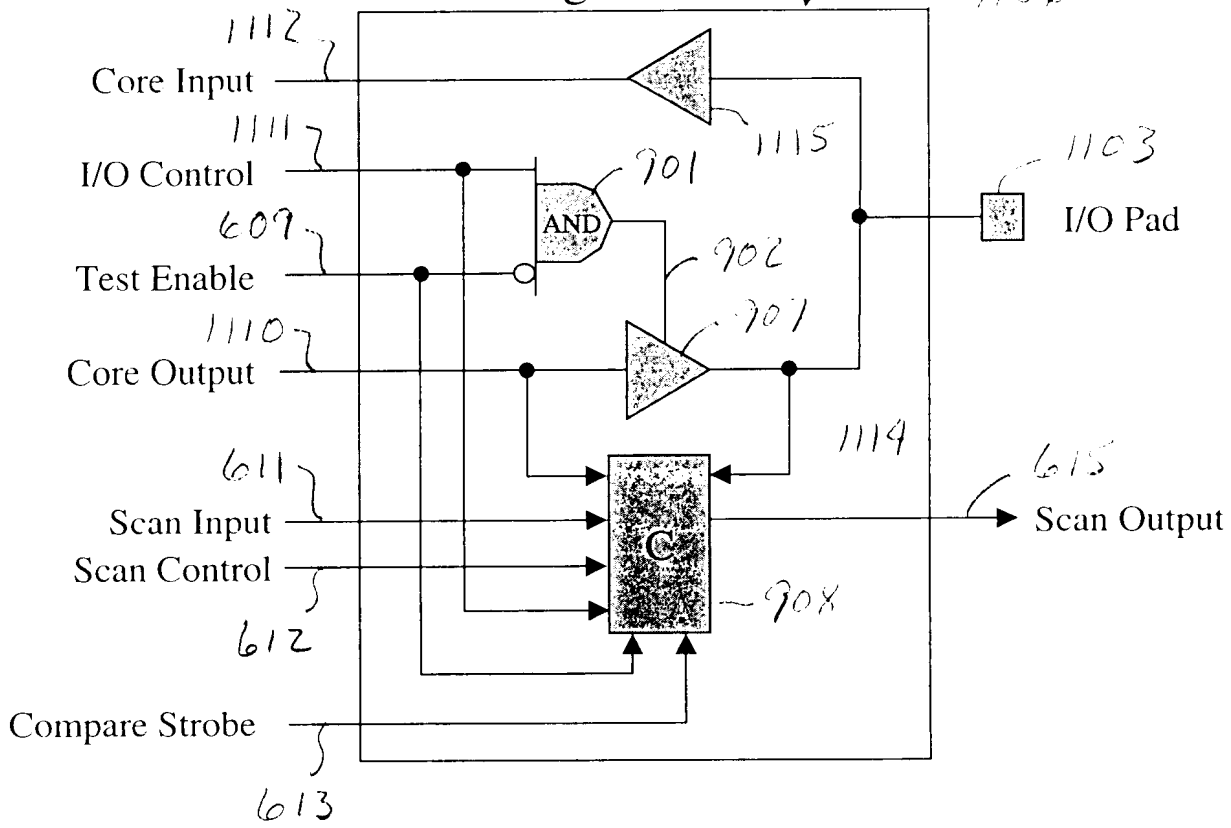


Figure 11B



Maskable Comparator For Input/Outputs

Figure 12A

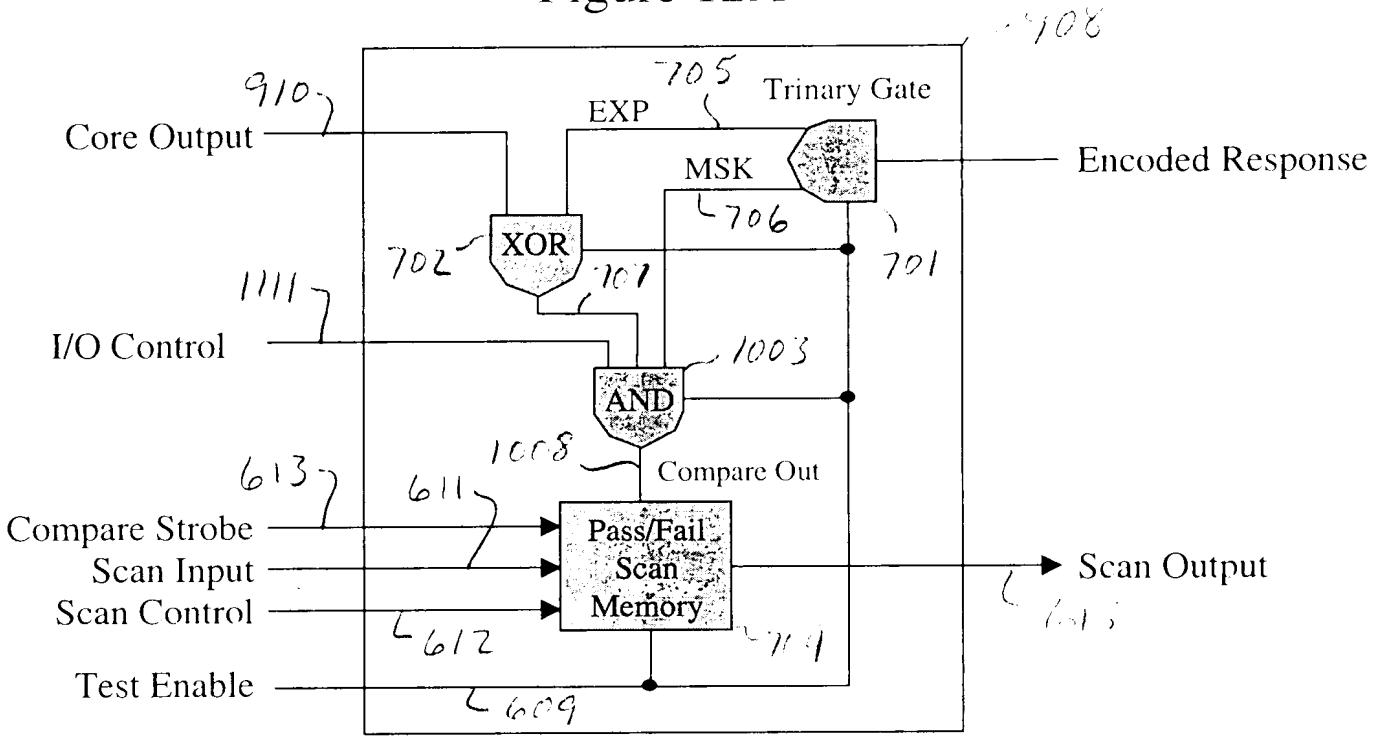


Figure 12B

IOC	TEN	ENR	MSK	EXP	Function Performed
X	0	X	X	X	Test Disabled
1	1	Gnd	1	0	Compare Low
1	1	Vdd	1	1	Compare High
1	1	1/2Vdd	0	X	Mask Compare
0	1	Gnd/Vdd	1	0/1	Test I/O Control
0	1	Gnd/Vdd	1	0/1	Input Stimulus

Fail Output for Diagnostic Testing

Figure 13A

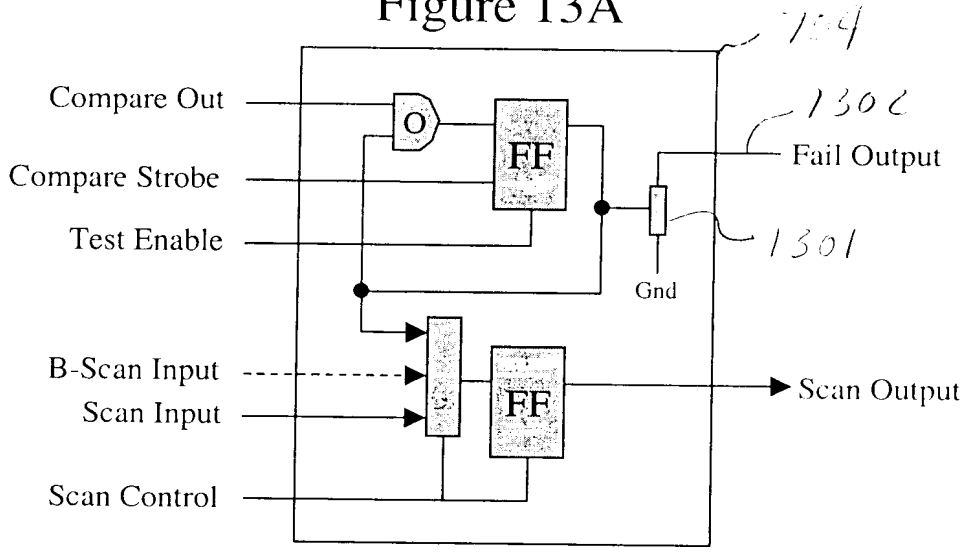
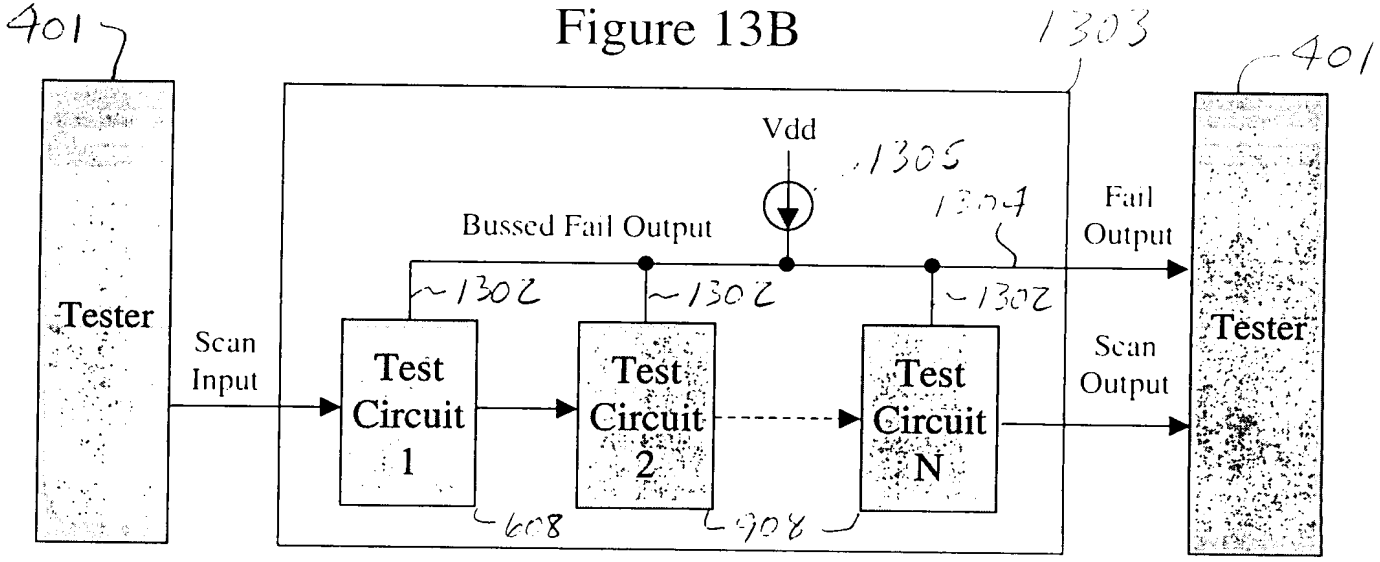
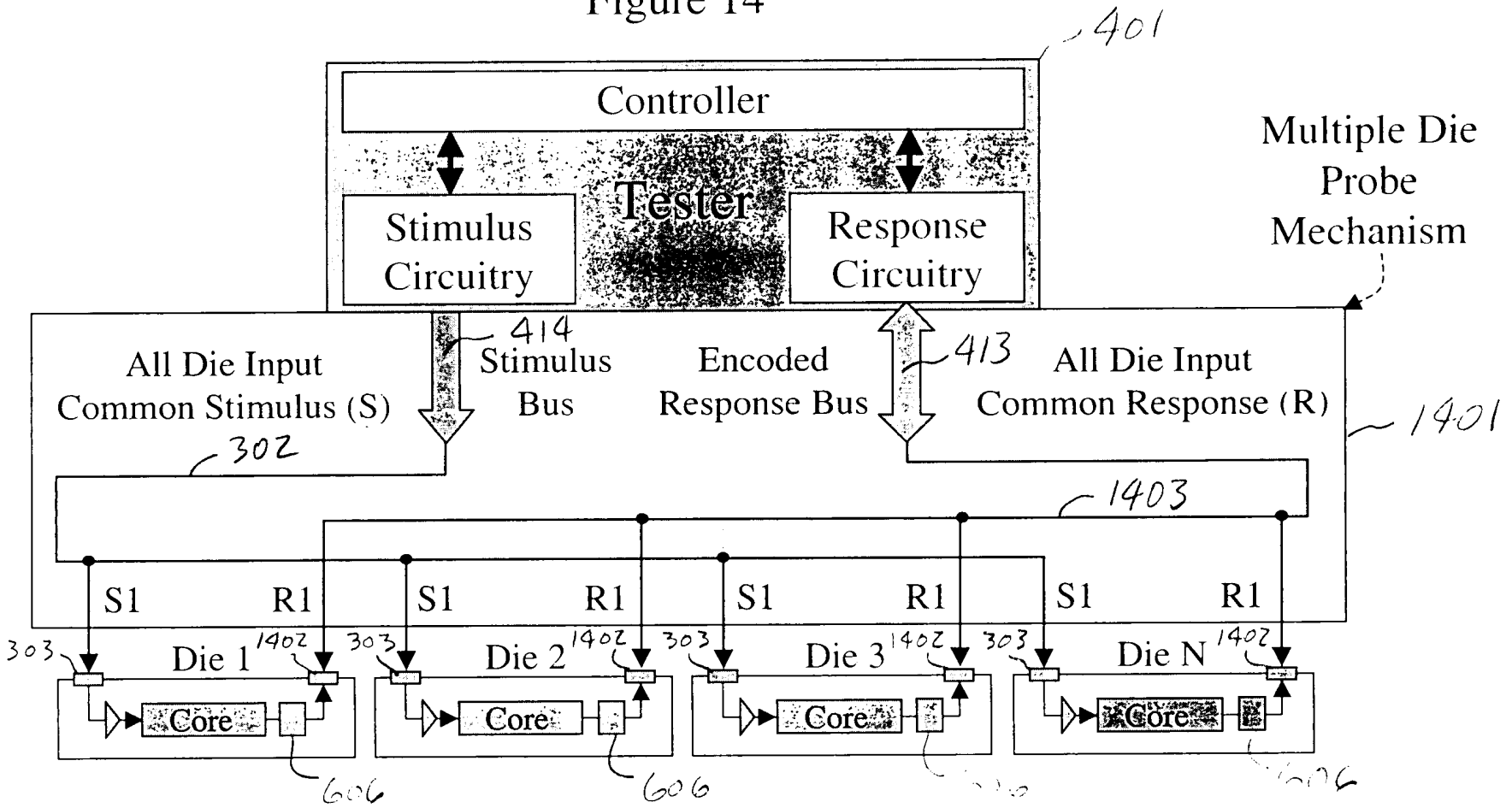


Figure 13B



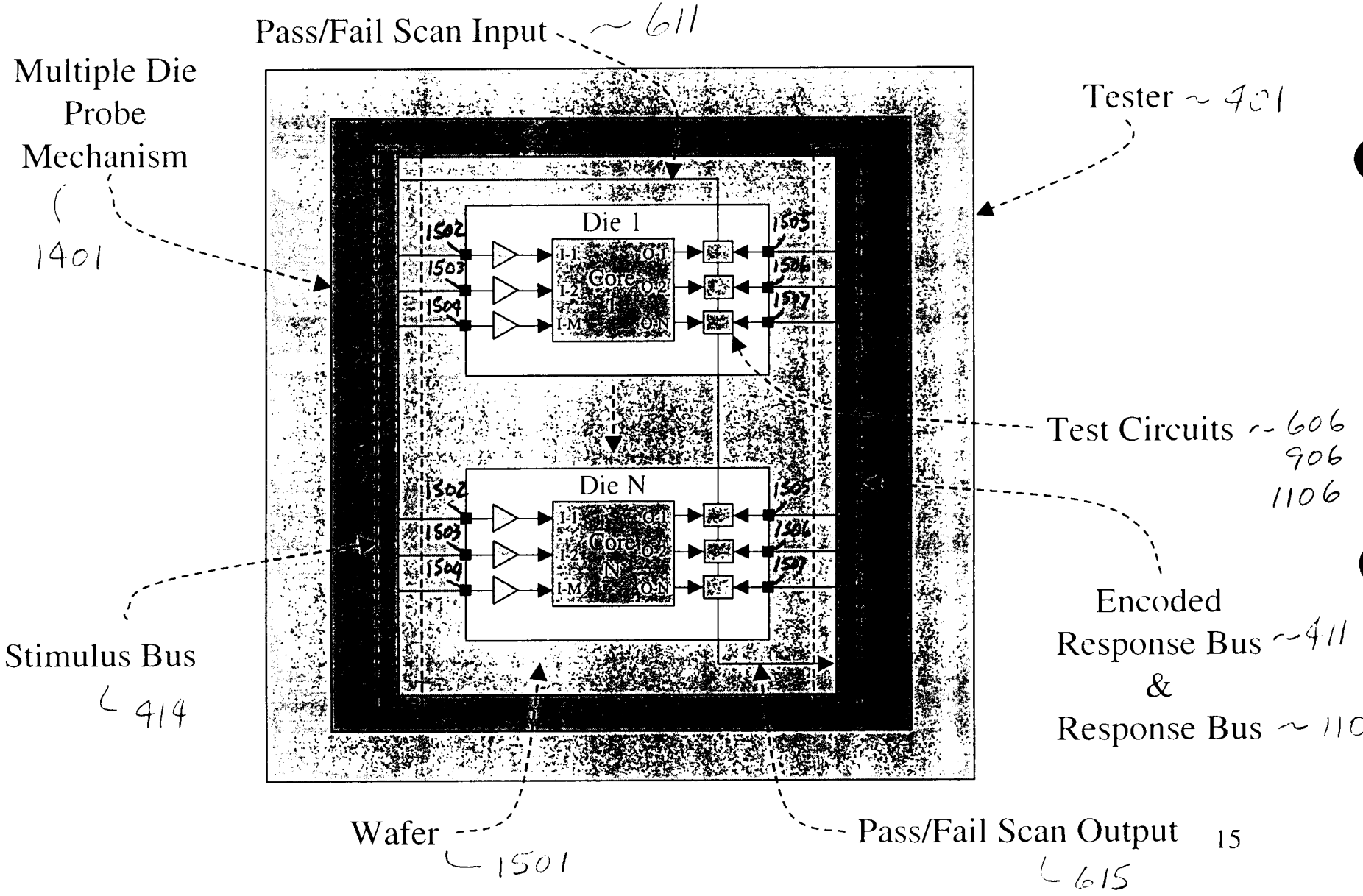
Improved Multiple Die Probe Test Example

Figure 14



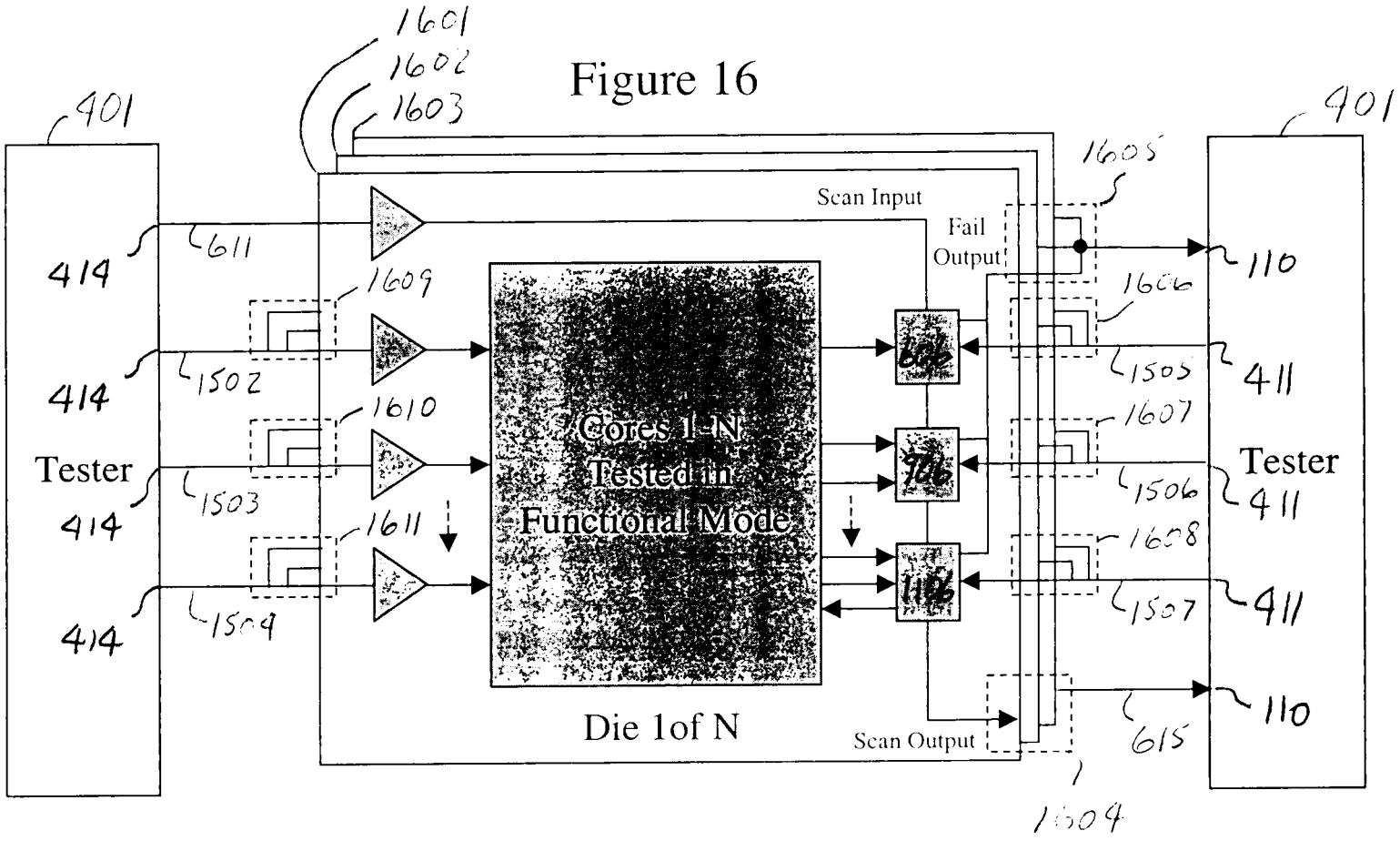
Conceptual View of Improved Die Test

Figure 15



Die Being Tested in Functional Mode

Figure 16



Die Being Tested in Scan Mode

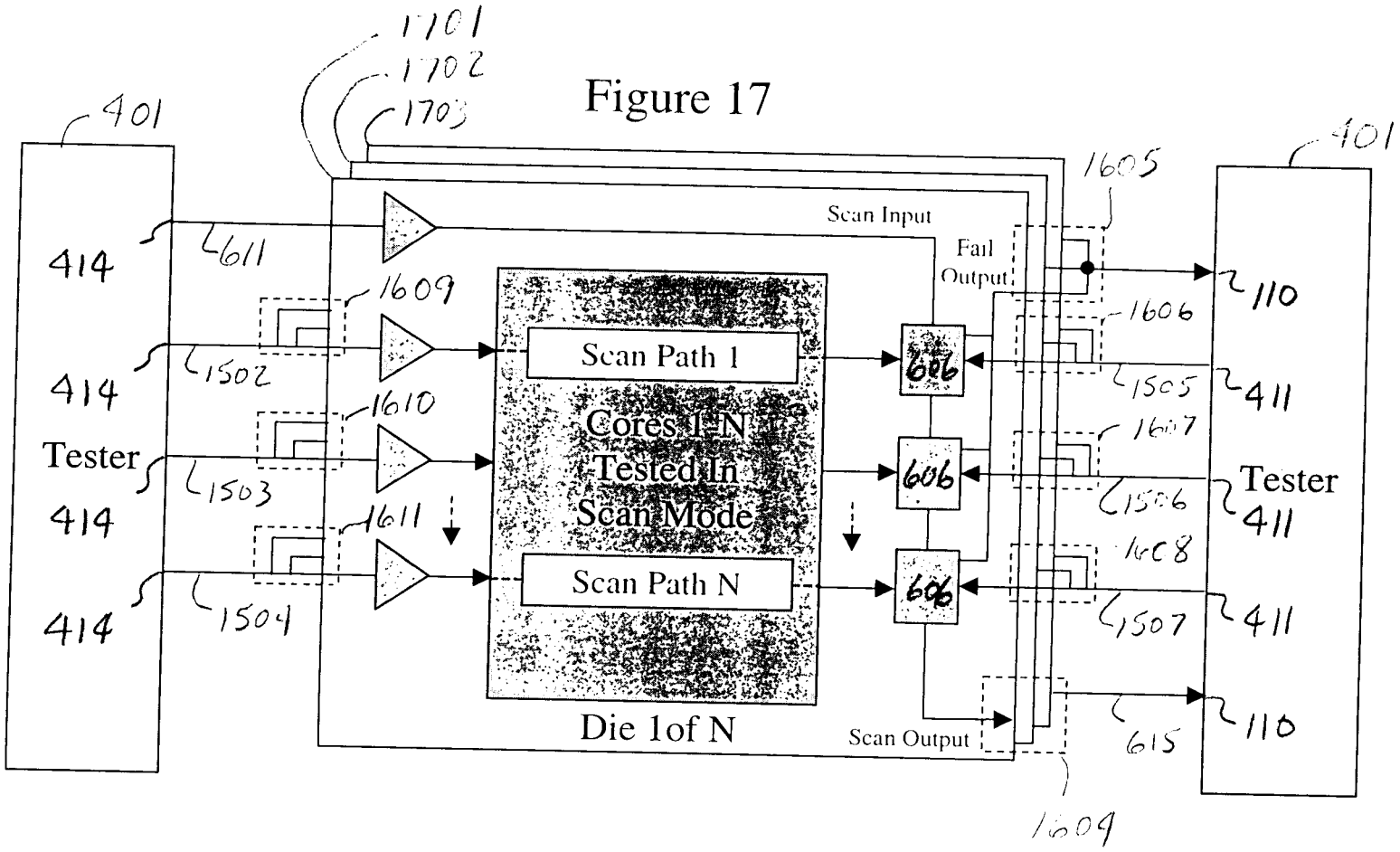


Figure 17

Testing System-On-Chip Die having
Multiple Embedded IP Core Sub-Circuits

Figure 18A

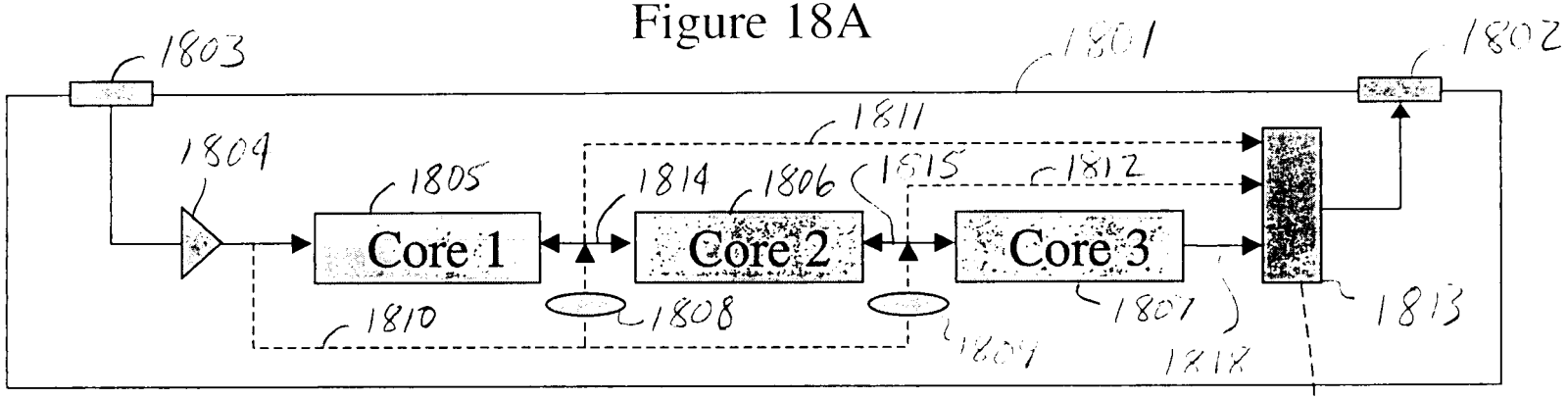


Figure 18B

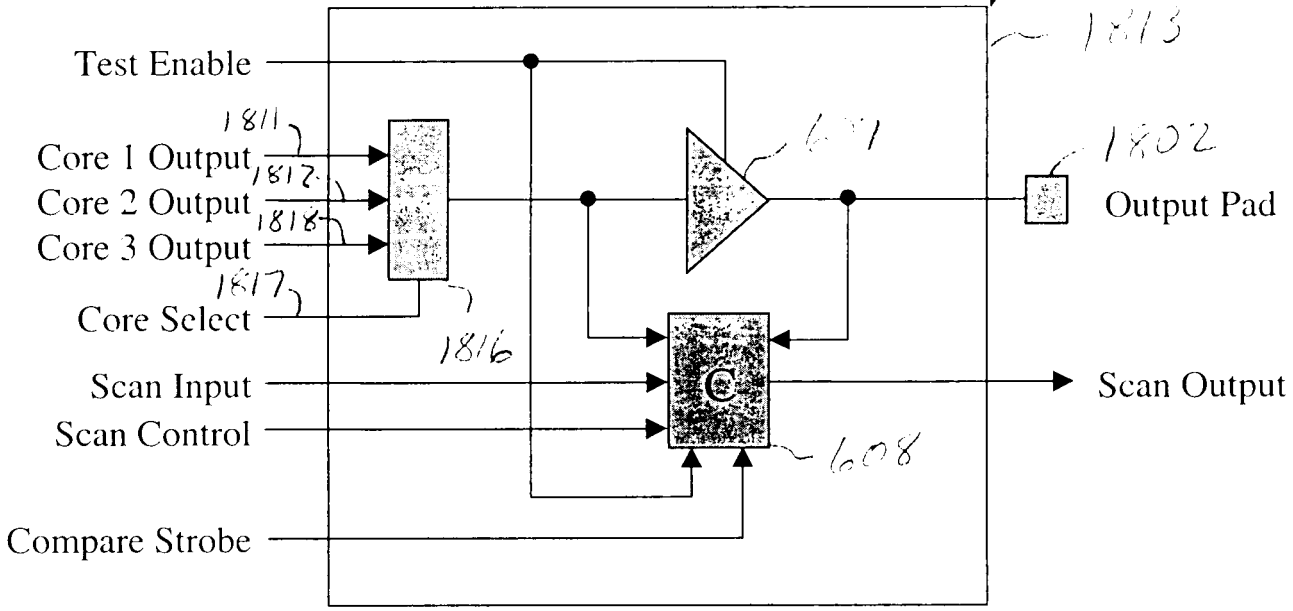
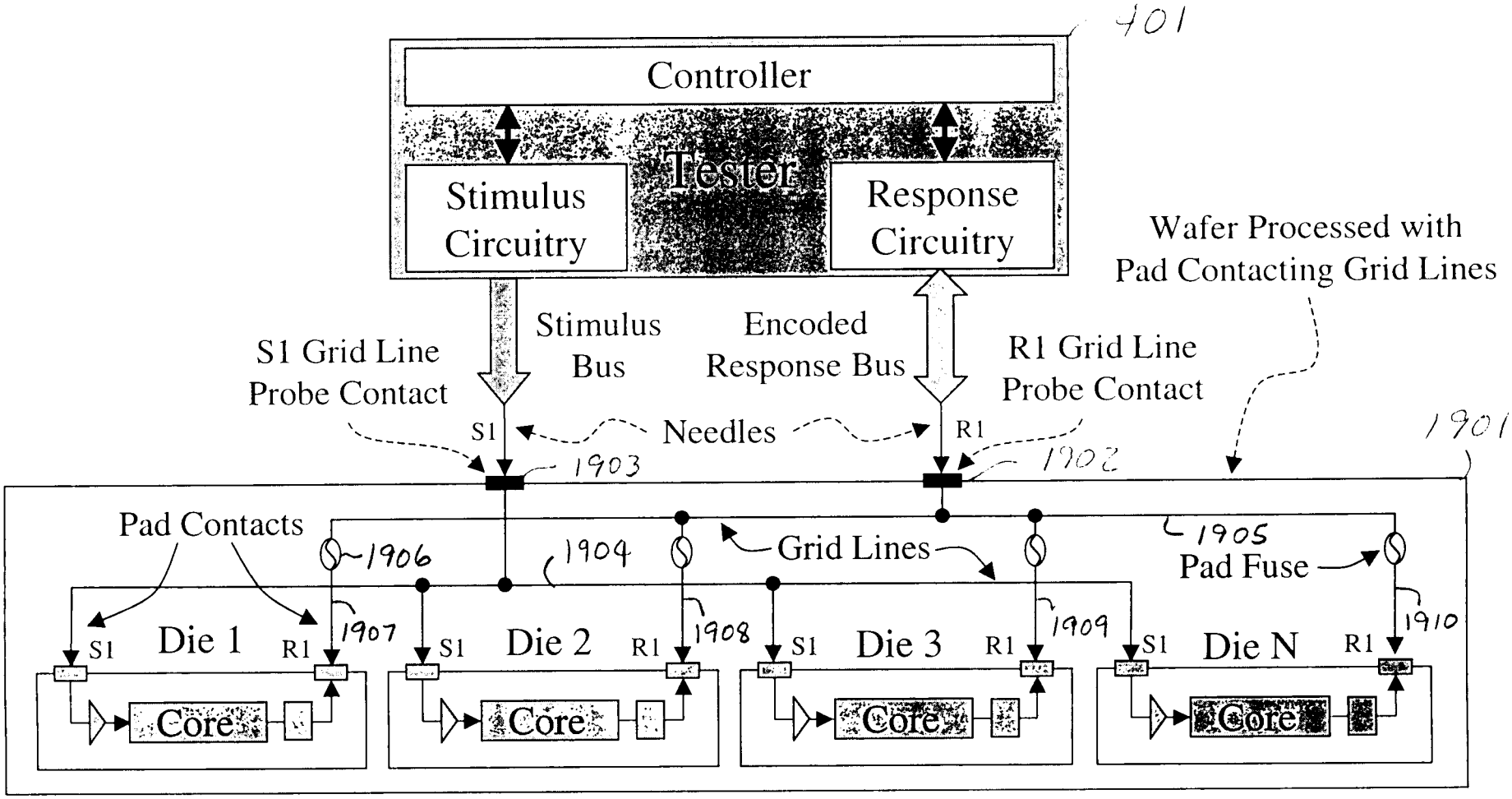
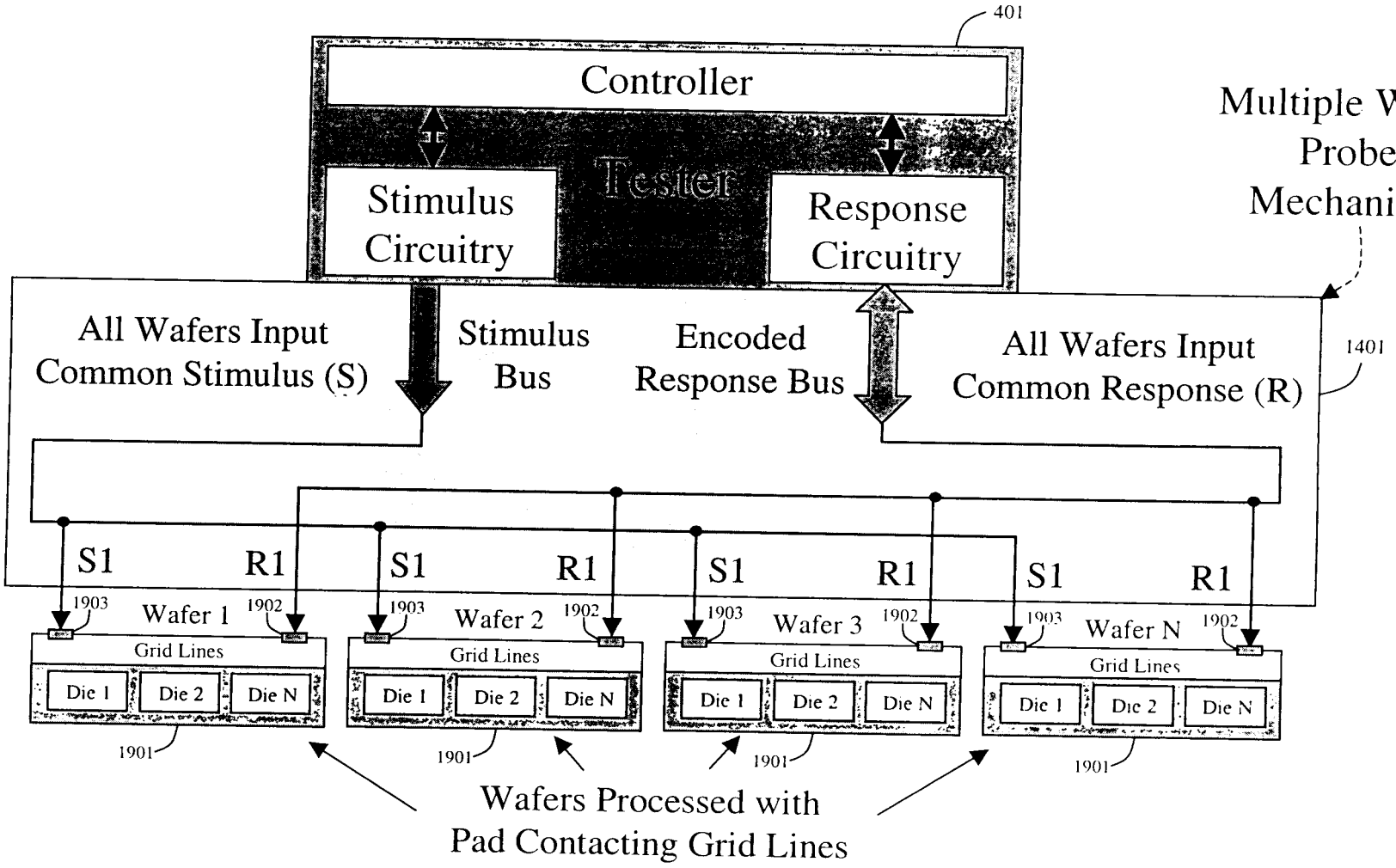


Figure 19


401
Controller
Tester
Stimulus Circuitry
Response Circuitry
Wafer Processed with Pad Contacting Grid Lines
Stimulus Bus
Encoded Response Bus
S1 Grid Line Probe Contact
R1 Grid Line Probe Contact
S1
Needles
R1
1903
1902
1901
Pad Contacts
1906
1904
Grid Lines
1905
Pad Fuse
1907
1908
1909
1910
S1
Die 1
R1
S1
Die 2
R1
S1
Die 3
R1
S1
Die N
R1
Core
Core
Core
Core

Improved Multiple Wafer Test Example

Figure 19A



Improved Multiple IC Test Example

Figure 20